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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,273	06/25/2003	Peter Brandt	31021037 US-01	4469

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EXAMINER	
DWIVEDI, MAHESH H	

ART UNIT	PAPER NUMBER
2168	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,273	BRANDT, PETER	
	Examiner	Art Unit	
	Mahesh H. Dwivedi	2168	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Receipt of Applicant's Amendment, filed on 06/05/2006, is acknowledged. The amended parts include amended the specification, the cancellation of claims 1-15, and the addition of claims 16-30.

Specification

2. The objections raised in the office action mailed on 02/01/2006 have been overcome by the applicant's amendment received on 06/05/2006.

Claim Rejections - 35 USC § 112

3. The objections raised in the office action mailed on 02/01/2006 have been overcome by the applicant's amendment received on 06/05/2006.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16-24, 26-27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Boner** (U.S. Patent 6,625,763) and in view of **Hemming** (U.S. PGPUB 2004/0168011).

6. Regarding claim 16 **Boner** teaches a method comprising:

A) Inputting a stream of data entities (Column 4, lines 54-57),

B) Writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written (Column 4, lines 54-65, Figure 2),

C) Performing selection and permutation on said memories (Column 8, lines 23-33, lines 35-39), and

D) Reading out said data entities in said permuted memories, in a memory-by-memory fashion (Column 8, lines 23-33, Figures 3-11).

The examiner notes that **Boner** teaches **"Inputting a stream of data entities"** as "RAM 100 receives and stores data bits D0-D127 as illustrated" (Column 4, lines 56-57). The examiner further notes that **Boner** teaches **"Writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written"** as "Data bits D0-D127 are sequentially ordered data bits, wherein D0 is the first bit of a data stream, and D127 is the last bit of the data stream" (Column 4, lines 57-59). The examiner further notes that **Boner** teaches **"Performing selection and permutation on said memories"** as "permutations in the column order can be accommodated, by changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39). The examiner further notes that the register file of **Boner** is a form of memory, and permutations are performed on the register file.

Boner does not explicitly teach:

E) Providing a number of memories equal to the maximum number of columns in the interleaver function.

Hemming, however, teaches **"Providing a number of memories equal to the maximum number of columns in the interleaver function"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hemming's** would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 17, **Boner** further teaches a method comprising:

A) wherein data entities in the input stream are first written into a register (Boner, Column 3, lines 40-45, Figures 3-11); and

B) when said register is filled, the step of writing into a memory is applied (Boner, Column 3, lines 40-45, Figures 3-11).

The examiner notes that **Boner** teaches **"wherein data entities in the input stream are first written into a register"** as "The register file is used for intermediate storage of the data values (bits or symbols) in a sequential input data stream. Data values to be written into the interleaver RAM are first written to the register file in column

order. Then the data values are transferred from the register file to the interleaver RAM in row order" (Column 3, lines 40-45). The examiner further notes that **Boner** teaches **"when said register is filled, the step of writing into a memory is applied"** as "The register file is used for intermediate storage of the data values (bits or symbols) in a sequential input data stream. Data values to be written into the interleaver RAM are first written to the register file in column order. Then the data values are transferred from the register file to the interleaver RAM in row order" (Column 3, lines 40-45).

Regarding claim 18, **Boner** further teaches a method comprising:

A) wherein said data entities are logical ones and zeros (Column 5, lines 17-19, Figure 2).

The examiner notes that Boner teaches **"wherein said data entities are logical ones and zeros"** as "a 4 column by 32 row RAM 200, which stored sequential data bits D0-D127 in a column order" (Column 5, lines 17-19). The examiner further notes that it is common knowledge that "data bits" (Column 5, lines 18) are in binary form.

Regarding claim 19, **Boner** further teaches a method comprising:

A) wherein said data entities are multiple bit words (Column 2, lines 31-45, Column 3, lines 40-45, Figures 3-11).

The examiner notes that Boner teaches **"wherein said data entities are multiple bit words"** as "If the SRAM block interleaver is arranged so that each row stores one or more memory words" (Column 2, lines 35-36).

Regarding claim 20, **Boner** further teaches a method comprising:

A) wherein said data entities are three bit words (Column 2, lines 43-45).

The examiner notes that Boner teaches **"wherein said data entities are three bit words"** as "assuming a word length of 3 bits (a full row), the block interleaver will be written during four cycles" (Column 2, lines 43-45).

Regarding claim 21, **Boner** further teaches a method comprising:

A) wherein said register is arranged to store each multiple bit word at one location in said memories (Column 3, lines 48-59.

The examiner notes that Boner teaches **"wherein said register is arranged to store each multiple bit word at one location in said memories"** as "the data values are written to the interleaver RAM in a row order, which is selected to implement a permutation of a column order of the original data stream" (Column 3, lines 49-52).

Regarding claim 22, **Boner** further teaches a method comprising:

A) wherein the number of columns used in the column interleaver function is changed on the fly, said number of columns not exceeding said maximum number of columns (Column 1, lines 54-60, Column 4, lines 14-19, lines 54-57).

The examiner notes that the interleaving function taught by **Boner** can be used for different bit sizes with accompanying columns.

Regarding claim 23 **Boner** teaches a method comprising:

A) means for implementing a column interleaving function (Column 3, lines 32-34);

B) means for inputting a stream of data entities (Column 4, lines 54-57),

C) means for writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written (Column 4, lines 54-65, Figure 2),

D) means for performing selection and permutation on said memories (Column 8, lines 23-33, lines 35-39), and

E) means for reading out said data entities in said permuted memories, in a memory-by-memory fashion (Column 8, lines 23-33, Figures 3-11).

The examiner notes that **Boner** teaches **"means for implementing a column interleaving function"** as "The present invention provides a block interleaver that includes a relatively small register file and a larger interleaver RAM" (Column 3, lines 32-34). The examiner further notes that **Boner** teaches **"means for inputting a stream of data entities"** as "RAM 100 receives and stores data bits D0-D127 as illustrated" (Column 4, lines 56-57). The examiner further notes that **Boner** teaches **"means for writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written"** as "Data bits D0-D127 are sequentially ordered data bits, wherein D0 is the first bit of a data stream, and D127 is the last bit of the data stream" (Column 4, lines 57-59). The examiner further notes that **Boner** teaches **"means for performing selection and permutation on said memories"** as "permutations in the column order can be accommodated, by

changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39). The examiner further notes that the register file of **Boner** is a form of memory, and permutations are performed on the register file.

Boner does not explicitly teach:

F) wherein the means for implementing the column interleaving function comprises: a number of memories equal to the maximum number of columns in the interleaving function.

Hemming, however, teaches **"wherein the means for implementing the column interleaving function comprises: a number of memories equal to the maximum number of columns in the interleaving function"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hemming's** would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 24, **Boner** teaches a module comprising:

A) A communication system device (Column 1, lines 14-20).

Regarding claim 26 **Boner** teaches a an integrated circuit device comprising:

A) a module for column interleaving, said module comprising means for implementing a column interleaving function (Column 3, lines 32-34);

B) means for inputting a stream of data entities (Column 4, lines 54-57),

C) means for writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written (Column 4, lines 54-65, Figure 2),

D) means for performing selection and permutation on said memories (Column 8, lines 23-33, lines 35-39), and

E) means for reading out said data entities in said permuted memories, in a memory-by-memory fashion (Column 8, lines 23-33, Figures 3-11).

The examiner notes that **Boner** teaches **"a module for column interleaving, said module comprising means for implementing a column interleaving function"** as "The present invention provides a block interleaver that includes a relatively small register file and a larger interleaver RAM" (Column 3, lines 32-34). The examiner further notes that **Boner** teaches **"means for inputting a stream of data entities"** as "RAM 100 receives and stores data bits D0-D127 as illustrated" (Column 4, lines 56-57). The examiner further notes that **Boner** teaches **"means for writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written"** as "Data bits D0-D127 are sequentially ordered data bits, wherein D0 is the first bit of a data stream, and D127 is the last bit of the data stream"

(Column 4, lines 57-59). The examiner further notes that **Boner** teaches **"means for performing selection and permutation on said memories"** as "permutations in the column order can be accommodated, by changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39). The examiner further notes that the register file of **Boner** is a form of memory, and permutations are performed on the register file.

Boner does not explicitly teach:

F) wherein the means for implementing the column interleaving function comprises: a number of memories equal to the maximum number of columns in the interleaving function.

Hemming, however, teaches **"wherein the means for implementing the column interleaving function comprises: a number of memories equal to the maximum number of columns in the interleaving function"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hemming's** would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 27, **Boner** teaches an integrated circuit comprising:

A) A communication system device (Column 1, lines 14-20).

Regarding claim 29 **Boner** teaches a column interleaver comprising:

A) means to perform column selection and permutation (Column 8, lines 23-33, lines 35-39), and

The examiner notes that **Boner** teaches **"means for performing selection and permutation on said memories"** as "permutations in the column order can be accommodated, by changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39). The examiner further notes that the register file of **Boner** is a form of memory, and permutations are performed on the register file.

Boner does not explicitly teach:

B) a number of memories equal to the maximum number of columns desired in the interleaver.

Hemming, however, teaches **"a number of memories equal to the maximum number of columns desired in the interleaver"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching

Hemming's would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 30, **Boner** further teaches a column interleaver comprising:

A) a register (Column 3, lines 40-45).

The examiner notes that **Boner** teaches **"a register"** as "The register file is used for intermediate storage of the data values (bits or symbols) in a sequential input data stream. Data values to be written into the interleaver RAM are first written to the register file in column order. Then the data values are transferred from the register file to the interleaver RAM in row order" (Column 3, lines 40-45).

7. Claims 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Boner** (U.S. Patent 6,625,763) and in view of **Hemming** (U.S. PGPUB 2004/0168011) as applied to claims 16-24, 26-27, and 29-30 and further in view of **Hustig et al.** (U.S. Patent 4,672,605).

8. Regarding claims 25, **Boner** and **Hemming** do not explicitly teach a module comprising:

A) A spread-spectrum communication apparatus

Hustig, however teaches "spread-spectrum communication apparatus" as "spread spectrum techniques" (Column 3, lines 38-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hustig's** would have allowed **Boner's** and **Hemming's** to provide error free communication, as noted by **Hustig** (Column 1, lines 55-57).

Regarding claims 28, **Boner** and **Hemming** do not explicitly teach an integrated circuit device comprising:

A) A spread-spectrum communication apparatus

Hustig, however teaches "spread-spectrum communication apparatus" as "spread spectrum techniques" (Column 3, lines 38-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hustig's** would have allowed **Boner's** and **Hemming's** to provide error free communication, as noted by **Hustig** (Column 1, lines 55-57).

Response to Arguments

9. Applicant's arguments filed on 06/05/2006 have been fully considered but they are not persuasive.

Applicant argues on page 6 that **"With respect to claims 16 through 30, applicant respectfully submits that Boner fails to disclose or suggest the feature of these claims of providing a number of memories equal to the maximum number of columns in the interleaving function"**. Applicant's arguments with

respect to claims 16-30 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues on page 9 that **"Boner discloses a number of columns equal to the length...Applicant respectfully disagrees"**. Applicant's arguments with respect to claims 16-30 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues on page 9 that **"includes the feature of the data entities in the input stream being written into a register and when the register is filled, the step of writing into a memory is applied. It is respectfully submitted that this feature cannot be found in Boner"**. However, the examiner wishes to point to Column 3 of **Boner**, and refer to the fifth paragraph which states **"The register file is used for intermediate storage of the data values (bits or symbols) in a sequential input data stream. Data values to be written into the interleaver RAM are first written to the register file in column order. Then the data values are transferred from the register file to the interleaver RAM in row order"** (Column 3, lines 40-45). The examiner wishes to state that **Boner's** method includes sending a stream to a register and then sending the stream to RAM after the register is filled.

Applicant argues on page 10 that **"claims 16 through 28 include the feature of performing selection and permutation on the memories...prior to writing to the single RAM memory"**. However, the examiner wishes to point to Column 8 of **Boner**, and refer to the third and fourth paragraphs which state **"permutations in the column order can be accommodated, by changing the manner in which data is**

transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and **"register file 301 can be implemented as a single-port RAM that can be written in column order"** (Column 8, lines 35-39). The examiner wishes to state that **Boner's** method includes performing permutation operations on memories since Boner defines a Register as being capable of becoming a RAM. The examiner further wishes to state that according to the limitation in claims 16-28, performing permutations on the register file is analogous to performing permutations on a memory.

Applicant argues on page 11 that **"In claim 19 the feature is disclosed of data entities...RAM concept cannot accept multiple-bit words"**. However, the examiner wishes to point to Column 2 of **Boner**, and refer to the fifth paragraph which states **"If the SRAM block interleaver is arranged so that each row stores one or more memory words"** (Column 2, lines 35-36). The examiner further wishes to state that **Boner's** method includes words having multiple bits in each word.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,954,885 issued to **Hurt et al.** on 11 October 2005. The subject matter disclosed therein is pertinent to that of claims 1-15 (e.g., methods interleave data)

U.S. Patent 6,061,820 issued to **Nakakita et al.** on 09 May 2000. The subject matter disclosed therein is pertinent to that of claims 1-15 (e.g., methods interleave data).

U.S. Patent 6,631,491 issued to **Shibutani et al.** on 07 October 2003. The subject matter disclosed therein is pertinent to that of claims 1-15 (e.g., methods interleave data).

U.S. Patent 4,291,406 issued to **Bahl et al.** on 22 September 1981. The subject matter disclosed therein is pertinent to that of claims 1-15 (e.g., methods interleave data).

U.S. Patent 4,394,642 issued to **Currie et al.** on 19 July 2003. The subject matter disclosed therein is pertinent to that of claims 1-15 (e.g., methods interleave data).

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahesh Dwivedi whose telephone number is (571) 272-2731. The examiner can normally be reached on Monday to Friday 8:20 am – 4:40 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached (571) 272-3642. The fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mahesh Dwivedi

Patent Examiner

Art Unit 2168

August 18, 2006

Leslie Wong

Primary Examiner